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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,334	03/12/2004	Aurel von Campenhausen	0928.0038C	6119

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EXAMINER	
GOLDEN, JAMES R	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 04/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,334	CAMPENHAUSEN ET AL.	
	Examiner	Art Unit	
	James Golden	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/30/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The instant application 10/798334 has a total of 7 claims pending. There are 2 independent claims and 5 dependent claims.

Information Disclosure Statement

1. The information disclosure statement submitted on 04/30/2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Objections

3. **Claims 2-4** are objected to because of the following informalities: "the memory further having and has..." (claim 2, line 3). Claims 3-4 are objected to because of their dependence on claim 2. These objections can be overcome by correcting line 3 of claim 2 to read --the memory further has...--.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1-7** are rejected under 35 U.S.C. 102(b) as being anticipated by Nakaoka (US 6,349,064).

6. **With respect to claim 1**, Nakaoka disclose an integrated memory, comprising:

- a plurality of memory cells (column 5, lines 34-37) in a memory cell array (100.0-100.3 of Fig. 1, 100n of Fig. 3; column 5, lines 34-37), the memory cells being combined to form individually addressable normal units (column 5, lines 38-42);
- a plurality of redundant units of memory cells (crosshatched pieces of 100.0-100.3 of Fig. 1; 100RC, 100RRC, 100RR of Fig. 3; column 8, lines 38-41) for respectively replacing one of the normal units on an address basis (column 6, lines 37-42);
- a memory unit (spare row decoder 112 of Fig. 2) for storing, in a normal mode (column 6, lines 37-42), an address for one of the normal units which needs to be replaced by one of the redundant units (fuses F11-F18 of redundancy determining units 2000.0-2000.3 of spare row decoder 112 of Fig. 2; column 1, lines 57-63; column 7, lines 46-48);
- a comparison unit (redundancy units 2000.0-2000.3 of Fig. 3; column 6, lines 37-42), the comparison unit being connected to an address bus in the memory (2000.0-2000.3 of Fig. 2 are part of 112 of Fig. 1, as in column 6, lines 26-27, and 2000.0-2000.3 are connected to 32 of Fig. 1,

an I/O bus as in column 6, lines 5-7, and the I/O bus receives addresses from 2 of Fig. 1, as in column 5, lines 43-45) and to an output of the memory unit (internal to 2000.0-2000.3 of Fig. 2) for the purpose of comparing an address which is present on the address bus with an address stored in the memory unit (column 15, lines 25-29) and for the purpose of activating one of the redundant units in the event of a match being identified (column 15, line 35 -- column 16, line 6); and

- a test circuit (112 of Fig. 1; column 6, lines 43-48), the test circuit being activated by a test mode signal (column 5, lines 60-65), and the test circuit adapted to reset the memory unit to an initial state (column 6, lines 26-42) and to store an address for one of the redundant units in the memory unit for subsequently writing to the redundant unit (column 6, line 31, "the stored defective address").

7. **With respect to claim 2**, Nakaoka disclose the integrated memory as claimed in claim 1 (see above paragraph 6), wherein the memory unit (112 of Fig. 1) is programmable (fuses F11-F18 of redundancy determining units 2000.0-2000.3 of spare row decoder 112 of Fig. 2; column 7, lines 46-48), the memory has a second nonvolatile memory unit (any of 2000.0-2000.3 of Fig. 2) for permanently storing an address (column 1, lines 57-63; column 7, lines 46-48), the memory further having at least one output which is connected to a corresponding input of the memory unit for transmitting an address stored in the second memory unit to the programmable memory unit (output SRD line

of 2000.0-2000.3 internal to and therefore connected to 112 of Fig. 2; column 6, lines 43-48).

8. **With respect to claim 3**, Nakaoka disclose the integrated memory as claimed in claim 2 (see above paragraph 7), wherein the second nonvolatile memory unit can be programmed only once (column 1, lines 36-38; column 7, lines 46-48; if the memory is programmed "by blowing off fuse elements" it cannot be programmed again).

9. **With respect to claim 4**, Nakaoka disclose the integrated memory as claimed in claim 2 (see above paragraph 7), wherein the second nonvolatile memory unit has laser fuses, which can be programmed from outside the memory by a laser beam (column 1, lines 34-38).

10. **With respect to claim 5**, Nakaoka disclose the integrated memory as claimed in claim 1 (see above paragraph 6), wherein the memory is in the form of a DRAM (column 5, lines 26-33).

11. **With respect to claim 6**, Nakaoka disclose the integrated memory as claimed in claim 1 (see above paragraph 6), wherein the memory unit is in the form of a register having register elements for storing a respective address bit (fuses F11-F18 of Fig. 2; column 1, lines 57-63; column 7, lines 46-48; these fuses meets the definition from The Authoritative Dictionary of IEEE Standards Terms, which defines a register as "a device capable of retaining information, often that contained in a small subset... of the aggregate information in a digital computer").

12. **With respect to claim 7**, Nakaoka disclose a method for testing an integrated memory, the integrated memory having

- a plurality of memory cells (column 5, lines 34-37) in a memory cell array (100.0-100.3 of Fig. 1, 100n of Fig. 3; column 5, lines 34-37), the memory cells being combined to form individually addressable normal units (column 5, lines 38-42),
- a plurality of redundant units of memory cells (crosshatched pieces of 100.0-100.3 of Fig. 1; 100RC, 100RRC, 100RR of Fig. 3; column 8, lines 38-41) for respectively replacing one of the normal units on an address basis (column 6, lines 37-42),
- a memory unit (spare row decoder 112 of Fig. 2) for storing, in a normal mode (column 6, lines 37-42), an address for one of the normal units which needs to be replaced by one of the redundant units (fuses, F11-F18 of redundancy determining units 2000.0-2000.3 of spare row decoder 112 of Fig. 2; column 1, lines 57-63; column 7, lines 46-48),
- a comparison unit (redundancy units 2000.0-2000.3 of Fig. 3; column 6, lines 37-42) which is connected to an address bus in the memory (2000.0-2000.3 of Fig. 2 is part of 112 of Fig. 1, as in column 6, lines 26-27, and 2000.0-2000.3 is connected to 32 of Fig. 1, an I/O bus as in column 6, lines 5-7, and the I/O bus receives addresses from 2 of Fig. 1, as in column 5, lines 43-45) and to an output of the memory unit (internal to 2000.0-2000.3 of Fig. 2) for the purpose of comparing an address which is present on the address bus with an address stored in the memory unit

(column 15, lines 25-29) and for activating one of the redundant units in the event of a match being identified (column 15, line 35 -- column 16, line 6),

the method comprising:

- activating a test mode (column 5, lines 60-65; column 6, lines 43-48);
- resetting the memory unit (112 of Fig. 2) to an initial state (column 6, lines 26-42);
- storing an address for one of the redundant units in the memory unit (column 6, line 31, "the stored defective address");
- writing an identification code to the one of the redundant units (column 16, lines 9-12);
- deactivating the test mode (column 11, lines 65-67);
- setting the memory unit using the address for one of the normal units which needs to be replaced (column 6, lines 37-42);
- accessing the memory cell array (column 15, lines 21-22, lines 30-34);
- applying addresses for normal units to the address bus for reading the memory cell array (column 15, lines 21-22, lines 30-34);
- reading the memory cell array (column 15, line 35 -- column 16, line 6); and
- associating the identification code which is read with the address for the normal unit addressed for this reading operation (column 11, line 67 -- column 12, line 3; column 16, lines 9-16).

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Nishikawa (US 5,848,003) teaches a redundant memory array that stores the addresses of faulty cells;
- Kim et al. (US 5,808,948) teach a redundant memory array with a test mode; and
- Lee et al. (US 5,732,029) also teach a redundant memory array with a test mode.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James R. Golden whose telephone number is 571-272-5628. The examiner can normally be reached on Monday-Friday, 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James R. Golden
Patent Examiner
Art Unit 2187

March 31, 2006

Primary Examiner
AU 2187
4/3/06